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Description

METHOD FOR FABRICATING A SEMICONDUCTOR TRANSISTOR DEVICE HAVING ULTRA-SHALLOW SOURCE/DRAIN EXTENSIONS

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention generally relates to semiconductor processes, and more particularly, to a method for fabricating a semiconductor transistor device having ultra-shallow source/drain extensions, which is capable of retarding silicon defect-induced transient enhanced diffusion (TED) effect.

[0003] 2. Description of the Prior Art

[0004] Continued device scaling demands that source/drain (S/D) junctions of MOS transistor devices become thinner and thinner to avoid short channel effect. However, the prior art MOS structure has a drawback in that the shallower the

S/D extension is, the greater the sheet resistance occurs in operation. As known to those skilled in the art, large sheet resistance leads to insufficient saturation currents. The situation becomes worse when the MOS device is a PMOS device. As silicon devices are continuously scaled to smaller sizes, there is an ever demand to reduce the diffusion of dopants. Diffusion mechanism and electrical activation of implanted dopant species such as B^+, P^+, and As^+dopants in crystalline Si are becoming essential to the fabrication of advanced nano-scale transistor devices.

[0005] Current methods for forming ultra-shallow junctions in the source and drain regions of complementary metal-oxide semiconductor (CMOS) transistor circuits use low energy ion implantation and rapid thermal annealing (RTA). Spike annealing, with fast ramping and short dwell time at maximum temperature, has been shown to be advantageous for shallow junction formation. During annealing, the implanted dopants such as boron experience an enhanced diffusion when excess Si interstitials are present. For implanted dopant species excess Si interstitials evolve from the residual implant damage until the damage is annealed out. The resulting enhanced diffusion is thus transient and is denoted transient-enhanced diffusion, or

TED, which adversely affects the performance of the transistor devices. It is generally accepted that boron diffuses primarily via an interstitial mechanism and boron diffusivity is, therefore, dependent on the silicon interstitial concentration.

[0006] In most cases, ultra-shallow source/drain extensions having low sheet resistance and abrupt junction profile are desired in terms of device's performance. Accordingly, there is a need in this industry to provide a method for fabricating a semiconductor transistor device having ultra-shallow source/drain extensions, which is capable of retarding silicon defect-induced transient enhanced diffusion (TED) effect, and thus reducing sheet resistance of the ultra-shallow source/drain extensions.

SUMMARY OF INVENTION

[0007] It is therefore the primary object of the present invention to provide a semiconductor process for eliminating or retarding the above-described silicon defect-induced transient enhanced diffusion effects.

[0008] It is another object of the present invention to provide a method for fabricating a semiconductor transistor device having ultra-shallow source/drain extensions, which is capable of retarding silicon defect-induced transient en-

hanced diffusion (TED) effect, and thus reducing sheet resistance of the ultra-shallow source/drain extensions.

[0009] It is still another object of the present invention to provide a method for fabricating a semiconductor transistor device having ultra-shallow source/drain extensions by utilizing a spacer layer having compressive residual stress.

[0010] According to the claimed invention, a method for fabricating a semiconductor transistor device having ultra-shallow source/drain extensions is provided. A silicon substrate having thereon a poly gate structure is prepared. The poly gate structure has sidewalls and a top surface. An offset spacer is formed on its sidewall. An ion implantation process is carried out to form an ultra-shallow junction doping region in the silicon substrate next to the offset spacer. An oxide liner is deposited on the offset spacer and on the top surface of the poly gate structure. A tensile nitride spacer layer is then deposited on the oxide liner. A stress modification implantation process is performed to turn the tensile nitride spacer layer into a less tensile stress status, or even into a compressive stress status. A dry etching process is then carried out to etch the nitride spacer layer so as to form a spacer.

[0011] Other objects, advantages, and novel features of the

claimed invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Brief Description of Drawings

[0012] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0013] Fig.1 to Fig.3 are schematic cross-sectional diagrams illustrating several intermediate steps for forming a PMOS field effect transistor device having ultra-shallow source/drain extensions in accordance with one preferred embodiment of this invention;

[0014] Fig.4 demonstrates a table listing preferred parameters of the stress modification implantation process using respective germanium and xenon as dopant; and

[0015] Fig.5 is a table listing changes to the stress of the nitride spacer layer and the sheet resistance (Rs) of the ultra-shallow source/drain extensions under different doping conditions when using germanium (Ge) as dopant during the stress modification implantation process.

DETAILED DESCRIPTION

[0016] Please refer to Fig.1 to Fig.3. Fig.1 to Fig.3 are schematic cross-sectional diagrams illustrating several intermediate steps for forming a PMOS field effect transistor device 100 having ultra-shallow source/drain extensions 18 in accordance with one preferred embodiment of this invention. As shown in Fig.1, an N type doped silicon substrate 10 is prepared. An exemplary active area 120 is defined by shallow trench isolation (STI) region. A poly gate structure 12 is formed on the active area 120. A gate dielectric such as silicon dioxide is interposed between the poly gate structure 12 and the silicon substrate 10.

[0017] An offset spacer 16 is formed on each sidewall of the poly gate structure 12. The offset spacer 16 is typically made of silicon dioxide, but not limited thereto. After the formation of the offset spacer 16, a low-energy ion implantation is performed to implant P type dopants such as boron into the silicon substrate 10 adjacent to the poly gate structure 12, thereby forming P type doping regions 18 having an ultra shallow junction. According to the preferred embodiment, the P type doping regions 18 has a junction depth that is less then 30 angstroms.

[0018] Subsequently, a chemical vapor deposition (CVD) process

or silicon oxide forming process using a furnace system is carried out to form a silicon dioxide liner 22 on the poly gate structure 12 and also on the P type doping regions 18. Preferably, the silicon dioxide liner 22 may use bis(tertiarybutylamine)silane (BTBAS) as a precursor.

[0019] A silicon nitride spacer layer 24 is then deposited on the silicon dioxide liner 22 using methods known in the art, for example, CVD methods. According to the preferred embodiment, the silicon nitride spacer layer 24 has a thickness of about 600~700 angstroms. At this phase, the silicon nitride spacer layer 24 has a tensile residual stress.

[0020] As shown in Fig.2, a stress modification implantation process 30 is carried out to alter the stress status inside the silicon nitride spacer layer 24. Preferably, dopant species that is electrically neutral and has a heavier atomic weight are used, for example, germanium or xenon. The preferred implantation energy of the stress modification implantation process 30 ranges between 25 and 150 KeV and the preferred dose of the stress modification implantation process 30 ranges between 2E14 and 5E15atoms/cm^2. After performing the stress modification implantation process, the implanted silicon nitride spacer layer 24 is turned into a less tensile status, or even into a

completely compressive status.

[0021] In accordance with the preferred embodiment, the stress modification implantation process 30 has a projected range (Rp) that is preferably smaller than the thickness of the silicon nitride spacer layer 24. By way of example, in a case that the thickness of the silicon nitride spacer layer 24 is about 700 angstroms, the projected range (Rp) of the stress modification implantation process 30 preferably ranges between 350 and 700 angstroms. Fig.4 demonstrates a table listing preferred parameters of the stress modification implantation process using respective germanium and xenon as dopant.

[0022] As shown in Fig.3, a dry etching process is performed to etch the silicon nitride spacer layer 24 so as to form a spacer 34 on each sidewall of the poly gate structure 12. Thereafter, an ion implantation process is carried out to implant P type dopants into the silicon substrate 10 adjacent to the spacer 34, thereby forming source/drain regions 48 of the PMOS transistor device 100.

[0023] Fig.5 is a table listing changes to the stress of the silicon nitride spacer layer 24 and the sheet resistance (Rs) of the ultra-shallow source/drain extensions 18 under different doping conditions when using germanium (Ge) as dopant

during the stress modification implantation process. As indicated, when a Ge implantation energy of 100 KeV and a implant dose of about 5E15atoms/cm^2 are used, the stress of the silicon nitride spacer layer 24 decreases from 1.19E10 dyne/cm^2 (tensile) down to -2.27E9 dyne/cm^2 (compressive), resulting in significant decrease of the sheet resistance of the ultra shallow junction doping regions from 4634ohm/sq down to 1787ohm/sq.

[0024] It is believed that the stress modification implantation process of the present invention is capable of reducing vacancy defects in the silicon surface because the stress status of the silicon nitride spacer layer 24 is altered from a tensile state to a compressive state. The defect-induced boron transient diffusion is thus alleviated. Hence, relative low sheet resistance and abrupt junction profile of the ultra-shallow source/drain extensions 18 are obtained.

[0025] Those skilled in the art will readily observe that numerous modifications and alterations of the present invention method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.